```
Set     Items   Description
S1    3919836   SIGNAL? ?
S2   18227440   TEST???? OR EXAMIN????? OR CHECK???? OR ANALY???? OR INSPE-
             CT???? OR EVALUAT?
S3   11873217   PLURALITY OR PLURAL? OR MULTIPL? OR CLUSTER? OR GROUP? OR -
             SEVERAL? OR MANY OR NUMEROUS? OR CONSIDERABL? OR PLENTY? OR A-
             RRAY?  OR MORE(W)THAN(W)ONE
S4    6180733   CABLE? OR LINES OR LINE OR WIRE? ? OR LEAD? ? OR BUS??
S5     313406   IMPEDANC???
S6    7560582   CONNECT? OR ATTACH? OR JOIN? OR BOND?
S7     527079   SERVER? OR NODE? ? OR (DISC OR DISK)(2N)(SUB()SYSTEM OR SU-
             BSYSTEM) OR (HOST? OR TARGET?)(2N)DEVICE?
S8     156072   (MEASUR? OR TEST?)(3N)(POINT? OR PTS OR CONNECT?)
S9     151600   S1(2N)S2
S10    201968   S3(3N)S4
S11      1262   S9 AND S10
S12       232   S9(10N)S10
S13         0   S12 AND S5 AND S6 AND S7 AND S8
S14       104   S9(3N)S10
S15     23347   S4 AND S6 AND S7
S16         1   S12 AND S15
S17      3489   S8 AND S9
S18        43   S9(N)S10
S19         4   S18 AND S5
S20         2   RD (unique items)
S21         2   S20 NOT S16
S22         0   S18 AND S6 AND S7
S23         0   S14 AND S6 AND S7
S24         1   S12 AND S6 AND S7
S25         0   S24 NOT (S16 OR S21)
S26      9703   S4(10N)S6(10N)S7
S27      7173   S4(6N)S6(6N)S7
S28        46   S27 AND S9
S29     68871   S1(N)S2
S30        21   S29 AND S27
S31        21   RD (unique items)
S32        20   S31 NOT (S16 OR S21)
? show files
File   2:INSPEC 1969-2002/Dec W3
         (c) 2002 Institution of Electrical Engineers
File   6:NTIS 1964-2002/Dec W5
         (c) 2002 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2002/Dec W4
         (c) 2002 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2002/Dec W5
         (c) 2002 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 144:Pascal 1973-2002/Dec W4
         (c) 2002 INIST/CNRS
File  35:Dissertation Abs Online 1861-2002/Nov
         (c) 2002 ProQuest Info&Learning
File  65:Inside Conferences 1993-2002/Dec W4
         (c) 2002 BLDSC all rts. reserv.
File  99:Wilson Appl. Sci & Tech Abs 1983-2002/Nov
         (c) 2002 The HW Wilson Co.
File  94:JICST-EPlus 1985-2002/Oct W3
         (c)2002 Japan Science and Tech Corp(JST)
File 347:JAPIO Oct 1976-2002/Aug(Updated 021203)
         (c) 2002 JPO & JAPIO
```

File 350:Derwent WPIX 1963-2002/UD,UM &UP=200282
(c) 2002 Thomson Derwent
?

16/9,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

03946022 **Image available**
CHANNEL TESTING SYSTEM

PUB. NO.: 04-311122 [JP 4311122 A]
PUBLISHED: November 02, 1992 (19921102)
INVENTOR(s): NOGI MASANOBU
APPLICANT(s): FUJI XEROX CO LTD [359761] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-103443 [JP 91103443]
FILED: April 09, 1991 (19910409)
INTL CLASS: [5] H04L-012/26; H04L-012/42; H04L-012/64
JAPIO CLASS: 44.3 (COMMUNICATION -- Telegraphy)
JOURNAL: Section: E, Section No. 1337, Vol. 17, No. 145, Pg. 33, March 24, 1993 (19930324)

ABSTRACT

PURPOSE: To more accurately execute a required channel test by allowing data for a channel test to pass a **line** exchange multiplexing part having a jitter filter part.

CONSTITUTION: Plural **nodes** M, N are mutually **connected** through a transmission **line** T, packet exchange communication and **line** exchange communication are multiplexed and constituted so as to attain both communication operation. Each of the **nodes** M, N is provided with a packet exchange transmission/ reception control part 9 and a **line** exchange **multiplexing** part 15 and a **test signal** sending part 7 and a test signal receiving part 8 are **connected** to the post stage of the multiplexing part 15 at the time of observing the **connection** from a transmission **line** T so as to allow required **line** exchange test data to pass the multiplexing part 15.

ABSTRACT

... execute a required channel test by allowing data for a channel test to pass a **line** exchange multiplexing part having a jitter filter part...

...CONSTITUTION: Plural **nodes** M, N are mutually **connected** through a transmission **line** T, packet exchange communication and **line** exchange communication are multiplexed and constituted so as to attain both communication operation. Each of the **nodes** M, N is provided with a packet exchange transmission/ reception control part 9 and a **line** exchange **multiplexing** part 15 and a **test signal** sending part 7 and a test signal receiving part 8 are **connected** to the post stage of the multiplexing part 15 at the time of observing the **connection** from a transmission **line** T so as to allow required **line** exchange test data to pass the multiplexing part 15.
?

21/9,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

5876894 INSPEC Abstract Number: B9805-7210B-031, C9805-7410H-039
Title: IEEE P1149.4-almost a standard
Author(s): Cron, A.
Author Affiliation: Motorola Inc., Schaumburg, IL, USA
Conference Title: Proceedings. International Test Conference 1997 (IEEE Cat. No.97CH36126) p.174-82
Publisher: Int. Test Conference, Washington, DC, USA
Publication Date: 1997 Country of Publication: USA xiv+1054 pp.
ISBN: 0 7803 4209 7 Material Identity Number: XX97-03053
U.S. Copyright Clearance Center Code: 0 7803 4209 7/97/$10.00
Conference Title: Proceedings International Test Conference 1997
Conference Sponsor: IEEE Comput. Soc. Test Technol. Tech. Committee; IEEE Philadelphia Sect.; IEEE
Conference Date: 1-6 Nov. 1997 Conference Location: Washington, DC, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: The IEEE P1149.4 Mixed- **Signal Test Bus** Working **Group** is on the cusp of delivering a document that will finally standardize the architecture for, and the method of access to, the analog portion of mixed-signal circuits for test and diagnostic applications. This Standard will have the same profound effect on the design and test community that IEEE 1149.1 had previously. P1149.4 gives the test infrastructure the capability to measure discrete **impedances** external to devices supporting the Standard using a 6-wire bus. This bus uses 4 of the same signals used today to support 1149.1 compliant devices and subsystems. This paper will detail the basic architecture; give some design-specific information and data learned through the Standard's development process; relate results from several test devices; and provide a basic example of usage. (13 Refs)
Subfile: B C
Descriptors: automatic test equipment; computer architecture; IEEE standards; integrated circuit testing; mixed analogue-digital integrated circuits; standardisation; system buses
Identifiers: IEEE P1149.4 standard; Mixed-Signal Test Bus; standardisation; mixed-signal circuits; diagnostic applications; test and diagnostic applications; test infrastructure; 6-wire bus; design
Class Codes: B7210B (Automatic test and measurement systems); B6210L (Computer communications); B2570 (Semiconductor integrated circuits); B1280 (Mixed analogue-digital circuits); C7410H (Computerised instrumentation); C5610S (System buses)
Copyright 1998, IEE

Abstract: The IEEE P1149.4 Mixed- **Signal Test Bus** Working **Group** is on the cusp of delivering a document that will finally standardize the architecture for...

... 1149.1 had previously. P1149.4 gives the test infrastructure the capability to measure discrete **impedances** external to devices supporting the Standard using a 6-wire bus. This bus uses 4...

21/9,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

02051907 INSPEC Abstract Number: A83054747, B83029613
Title: Cable tester

Author(s): Weiner, J.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.25, no.10 p.4950
Publication Date: March 1983 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: Describes a test fixture which solves the problem of **testing** **multiple** **signal** **wires** by **testing** all of the cable signal wires in series using time domain reflectometer which measures characteristic **impedance** of the cable. (0 Refs)
Subfile: A B
Descriptors: cables (electric); time-domain reflectometry
Identifiers: cable tester; characteristic **impedance** ; time domain reflectometer; multiple signal wires
Class Codes: A0750 (Electrical instruments and techniques); B2160 (Wires and cables); B7310N (Microwave techniques)

Abstract: Describes a test fixture which solves the problem of **testing** **multiple** **signal** **wires** by **testing** all of the cable signal wires in series using time domain reflectometer which measures characteristic **impedance** of the cable.
...Identifiers: characteristic **impedance** ;
?

32/9,K/10 **(Item 7 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

012040083 **Image available**
WPI Acc No: 1998-456993/199839
XRPX Acc No: N98-356660

Safety device for diagnostic terminals in distributed computer networks - Has signal evaluation circuit detecting signal state at set of contact pins to switch relays connecting diagnostic equipment

Patent Assignee: MECEL AB (MECE-N)
Inventor: FRIMODIG H; LUNDQVIST A; VAESTRA A L
Number of Countries: 003 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9835857	A1	19980820	WO 98SE268	A	19980213	199839	B
SE 9700546	A	19980818	SE 97546	A	19970217	199844	
DE 19880227	T	19990415	DE 1080227	A	19980213	199921	
			WO 98SE268	A	19980213		
SE 511458	C2	19991004	SE 97546	A	19970217	199947	
DE 19880227	C2	20010201	DE 1080227	A	19980213	200107	
			WO 98SE268	A	19980213		
US 6351828	B1	20020226	WO 98SE268	A	19980213	200220	
			US 98155387	A	19980928		

Priority Applications (No Type Date): SE 97546 A 19970217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9835857	A1	E	12	B60R-016/02	
Designated States (National): DE US					
SE 9700546	A			B60R-016/02	
DE 19880227	T			G06F-011/00	Based on patent WO 9835857
SE 511458	C2			B60R-016/02	
DE 19880227	C2			G06F-011/273	Based on patent WO 9835857
US 6351828	B1			G06F-011/30	Based on patent WO 9835857

Abstract (Basic): WO 9835857 A

Device is for a diagnostic terminal (3) in distributed computer networks (8) containing at least two **nodes** and a common communication **bus** (10a,10b) for **connecting** external diagnostic equipment (1) to distributed **nodes** (20a,20b,20c). Relay switches (14a,14b) are arranged between contact pins (3a,3b) and bus (10a,10b).

USE - Safety device is for diagnostic terminals in distributed computer networks used in vehicles for direct access to communication buses transmitting information between distributed nodes within the computer network during operation.

ADVANTAGE - Device prevents short-circuiting of the communications bus used in distributed computer networks if the contact pins in a diagnostic terminal connected to the bus should be short circuited. It prevents misapplication of voltages etc. on the bus, reduces the number of pins required in the diagnostic terminal and protects against unauthorised access via the terminal to the bus in distributed computer networks.

Dwg.1/5

Title Terms: SAFETY; DEVICE; DIAGNOSE; TERMINAL; DISTRIBUTE; COMPUTER; NETWORK; SIGNAL; EVALUATE; CIRCUIT; DETECT; SIGNAL; STATE; SET; CONTACT; PIN; SWITCH; RELAY; CONNECT; DIAGNOSE; EQUIPMENT
Derwent Class: Q17; T01; W01; X22
International Patent Class (Main): B60R-016/02; G06F-011/00; G06F-011/273; G06F-011/30
International Patent Class (Additional): G06F-013/00
File Segment: EPI; EngPI

Manual Codes (EPI/S-X): T01-H07C5; T01-J07C; W01-A06A1; W01-A06B1;
W01-A06B5A; X22-X

... **Has** signal evaluation **circuit detecting signal state at set of contact pins to switch relays connecting diagnostic equipment**

...Abstract (Basic): is for a diagnostic terminal (3) in distributed computer networks (8) containing at least two **nodes** and a common communication **bus** (10a,10b) for **connecting** external diagnostic equipment (1) to distributed **nodes** (20a,20b,20c). Relay switches (14a,14b) are arranged between contact pins (3a,3b) and...

32/9,K/14 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

009122104 **Image available**
WPI Acc No: 1992-249541/199230
XRPX Acc No: N92-190628
Disposable high performance test head - comprises signal platform including tape layer and interconnection lines coupled with test nodes
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: ATON T J; RINCON R M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5128612	A	19920707	US 90560404	A	19900731	199230	B

Priority Applications (No Type Date): US 90560404 A 19900731
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5128612	A		11	G01R-001/00	

Abstract (Basic): US 5128612 A

A disposable integrated circuit test head communicates **test signals** between test nodes of an integrated circuit and test circuitry. A high-density test head (30) comprises a signal platform which includes tape layer and interconnection lines, which include signal **leads** (30) and bumps (32). The **lines** are coupled with the test **nodes** to electrically **connect** test **nodes** with the test circuitry and communicate the **test signals** between the nodes and test circuitry.

A pusher block (36) engages the signal platform at the tape layer opposite interconnection lines and applies force through the tape layer to interconnection lines. This allows positive engagement of interconnection lines with the test nodes. The pusher block comprises rigid force applying plate (38) which adheres to compliant layer (40) at a junction. A compliant layer (40) absorbs planarity differences between the interconnection lines and integrated circuit test nodes.

USE - Disposable test head for use during integrated circuit manufacture.

Dwg. 4/11

Title Terms: DISPOSABLE; HIGH; PERFORMANCE; TEST; HEAD; COMPRISE; SIGNAL; PLATFORM; TAPE; LAYER; INTERCONNECT; LINE; COUPLE; TEST; NODE
Derwent Class: S01; U11
International Patent Class (Additional): G01R-001/04
File Segment: EPI
Manual Codes (EPI/S-X): S01-G02B; S01-H03; U11-F01C1; U11-F01C3
...Abstract (Basic): A disposable integrated circuit test head communicates

test signals between test nodes of an integrated circuit and test circuitry. A high-density test head (30) comprises a signal platform which includes tape layer and interconnection lines, which include signal **leads** (30) and bumps (32). The **lines** are coupled with the test **nodes** to electrically **connect** test **nodes** with the test circuitry and communicate the **test signals** between the nodes and test circuitry...

32/9,K/18 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

007303913
WPI Acc No: 1987-300920/198743
XRPX Acc No: N87-224797
Dense interconnected data transmission network - uses flow check signals **which is modified by each relevant node to provide continuous supervision of operating state**
Patent Assignee: SIEMENS AG (SIEI)
Inventor: MUELLER W; SCHNEIDER W; MULLER W
Number of Countries: 006 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 243297	A	19871028	EP 87730037	A	19870414	198743	B
DE 3614062	A	19871029	DE 3614062	A	19860423	198744	
US 4825208	A	19890425	US 8739432	A	19870417	198919	
EP 243297	B1	19920909	EP 87730037	A	19870414	199237	
DE 3781581	G	19921015	DE 3781581	A	19870414	199243	
			EP 87730037	A	19870414		

Priority Applications (No Type Date): DE 3614062 A 19860423
Cited Patents: 2.Jnl.Ref; A3...8933; No-SR.Pub; US 4475192; WO 8502964
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 243297	A	G	5		
Designated States (Regional): AT BE DE IT NL					
US 4825208	A		5		
EP 243297	B1	G	7	H04L-012/54	
Designated States (Regional): AT BE DE IT NL					
DE 3781581	G			H04L-012/54	Based on patent EP 243297

Abstract (Basic): EP 243297 A
The node points (C,..F) involved in connection for sending data, transmit cyclically, and in a predetermined sequence, certain data flow **check signals** (FCM...) The first **check signal** (FCM1) indicates the transmission of normal length data blocks. The second **check signal** (FCM2) is used if the amount of data for transmission exceeds the normal for the time cycle. The latter (FCM2) is transmitted by the intermediate nodes if there is no hold up due to data overload.
In the case of a hold up due to overload the data flow **check signals** are modified, and act, after determining the sending and receiving nodes (eg C,F), to block the relevant transmission memory (SS).
USE/ADVANTAGE - Data flow control is interlinked data networks. Flow **check signals** can be modified at any node point between originating and target nodes providing continuous supervision of the network.
1/1
Abstract (Equivalent): EP 243297 B

Method for the flow control of data which can be exchanged by users via nodes **connecting** origin and destination to one another, the **nodes** being **connected** to one another arbitrarily meshed via **lines** within a data network and each **node** being equipped with a transmission memory means and a reception memory means, characterised by the combination of the features: 1.1 the nodes (C... , F) participating in a connection cyclically transmit a first flow control signal (FCM1) in a longer time cycle than that which is defined depending on an average number of data items to be transmitted between two users via the longest connecting path within the data network, which flow control signal provides authorisation for receiving further quantities of data from the reception memory means (ES) of the respective upstream and/or downstream nodes (C.) by unchanged forwarding to the transmission memory means (SS) of the respective nodes (C.), 1.2 when required the nodes (C.) participating in the connection transmit a second flow control signal (FCM2) depending on a quantity of data exceeding the average number of data items to be transmitted within a time cycle, which flow control signal provides authorisation for receiving further quantities of data from the reception memory means (ES) of the respective upstream and/or downstream nodes (C.) by unchanged forwarding to the transmission memory means (SS) of the respective nodes (C.), 1.3 in the case of a jam in the reception memory means (ES) of the respective upstream and/or downstream nodes (C.), the first flow control signal (FCM1) and the second flow control signal (FCM2) are erased or are provided with an additional identifier and are sent back by means of the transmission memory means (SS) of the respective upstream and/or downstream nodes (C.) in receiving direction (reverse direction), and 1.4 in the nodes (C,F) forming origin and destination, the omission of the first and second flow control signals (FCM1,FCM2) erased in the case of a jam, or the reception of the first and second flow control signals (FCM1,FCM2) provided with the additional identifier in the case of a jam, within two time cycles causes the inhibition of the respective transmission memory means (SS), it being possible to switch the respective transmission memory means (SS) over from the `undisturbed' to the `jam has occurred' state. (Dwg.1/1)n

Abstract (Equivalent): US 4825208 A

The method includes the step of connecting an origin and a destination to one another. The nodes are arbitrarily meshed within a data network and are **connected** to one another via **lines** . Every **node** is equipped with a transmission memory and a reception memory device. The method also includes cyclical transmission of a first control signal (FCM1) in a prescribed time sequence and, as needed, a second control signal (FCM2) dependent on a data quantity within a time cycle which exceeds the quantity of data usually transmitted.

These control signals are forwarded to the respectively adjacent nodes in case of unimpeded data transmission. In the jam condition, these flow control signals (FCM1,FCM2) are omitted or modified and, after recognition by the respective nodes effect the inhibition of the corresponding transmission memory (SS) at such node. (5pp)o

Title Terms: DENSE; INTERCONNECT; DATA; TRANSMISSION; NETWORK; FLOW; CHECK; SIGNAL; MODIFIED; RELEVANT; NODE; CONTINUOUS; SUPERVISION; OPERATE; STATE
Derwent Class: W01
International Patent Class (Main): H04L-012/54
International Patent Class (Additional): G06F-013/14; H04L-011/20; H04L-025/02; H04Q-009/00; H04Q-011/04
File Segment: EPI
Manual Codes (EPI/S-X): W01-A06A; W01-A06B1

... **uses flow** check signals **which is modified by each relevant node to provide continuous supervision of operating state**

...Abstract (Basic): in connection for sending data, transmit cyclically, and in a predetermined sequence, certain data flow **check signals** (FCM...) The first **check signal** (FCM1) indicates the transmission of normal length data blocks. The second **check signal** (FCM2) is used if the amount of data for transmission exceeds the normal for the ...

...In the case of a hold up due to overload the data flow **check signals** are modified, and act, after determining the sending and receiving nodes (eg C,F), to...

...USE/ADVANTAGE - Data flow control is interlinked data networks. Flow **check signals** can be modified at any node point between originating and target nodes providing continuous supervision...

...Abstract (Equivalent): Method for the flow control of data which can be exchanged by users via nodes **connecting** origin and destination to one another, the **nodes** being **connected** to one another arbitrarily meshed via **lines** within a data network and each **node** being equipped with a transmission memory means and a reception memory means, characterised by the...

...Abstract (Equivalent): destination to one another. The nodes are arbitrarily meshed within a data network and are **connected** to one another via **lines** . Every **node** is equipped with a transmission memory and a reception memory device. The method also includes...

32/9,K/20 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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002177141
WPI Acc No: 1979-K7091B/197946
Automatic digital in-circuit tester contg. LSI circuits - has selectable switches with test signal **generators and central processor**
Patent Assignee: ZEHNTEL INC (ZEHN-N)
Inventor: GARRETT T C; RAYMOND D W
Number of Countries: 010 Number of Patents: 013
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2020439	A	19791114				197946	B
DE 2918053	A	19791115				197947	
NO 7901508	A	19791203				198001	
SE 7903873	A	19791210				198001	
FI 7901414	A	19791231				198004	
FR 2425078	A	19800104				198008	
DK 7901839	A	19800512				198023	
US 4216539	A	19800805				198034	
GB 2020439	B	19821215				198250	
CA 1141436	A	19830215				198311	
US 31828	E	19850205				198508	
IT 1116589	B	19860210				198725	
DE 2918053	C	19880310				198810	

Priority Applications (No Type Date): US 78903160 A 19780505

Abstract (Basic): GB 2020439 A

The tester uses a programmed processor which controls switches which **connect** selected **nodes** of circuit board under test to certain signal **lines** . One of the **lines** supplies a digital **test signal** from a selectable set of signals to the selected **node** . Another of the

signal **lines** provides a response **line connecting** a selected **node** to a functional tester which performs one of a selectable number of intermediate functional tests.

One of the functional tests is a signature analysis of the digital response signal in accordance with a cyclic redundancy check coding technique. Each test performed is specified through processor routines which select the proper **test signals** for the device under test, and the results are analysed to determine if the device is functioning properly.

Title Terms: AUTOMATIC; DIGITAL; CIRCUIT; TEST; CONTAIN; LSI; CIRCUIT; SELECT; SWITCH; TEST; SIGNAL; GENERATOR; CENTRAL; PROCESSOR
Derwent Class: S01
International Patent Class (Additional): G01R-031/28; G06F-011/00
File Segment: EPI

... has selectable switches with test signal **generators and central processor**

...Abstract (Basic): The tester uses a programmed processor which controls switches which **connect** selected **nodes** of circuit board under test to certain signal **lines** . One of the **lines** supplies a digital **test signal** from a selectable set of signals to the selected **node** . Another of the signal **lines** provides a response **line connecting** a selected **node** to a functional tester which performs one of a selectable number of intermediate functional tests...

...check coding technique. Each test performed is specified through processor routines which select the proper **test signals** for the device under test, and the results are analysed to determine if the device...

?

```
Set     Items   Description
S1     480044   SIGNAL? ?
S2    1568515   TEST???? OR EXAMIN????? OR CHECK???? OR ANALY???? OR INSPE-
             CT???? OR EVALUAT?
S3    1141466   PLURALITY OR PLURAL? OR MULTIPL? OR CLUSTER? OR GROUP? OR -
             SEVERAL? OR MANY OR NUMEROUS? OR CONSIDERABL? OR PLENTY? OR A-
             RRAY?  OR MORE(W)THAN(W)ONE
S4     873911   CABLE? OR LINES OR LINE OR WIRE? ? OR LEAD? ? OR BUS??
S5      46065   IMPEDANC???
S6    1077134   CONNECT? OR ATTACH? OR JOIN? OR BOND?
S7     101022   SERVER? OR NODE? ? OR (DISC OR DISK)(2N)(SUB()SYSTEM OR SU-
             BSYSTEM) OR (HOST? OR TARGET?)(2N)DEVICE?
S8      26035   (MEASUREMENT? OR TEST?)(3N)(POINT? OR PTS OR CONNECT?)
S9      11510   S1(N)S2
S10     79535   S3(2N)S4
S11      2408   S9 AND S10
S12       862   S11 AND S6 AND S7
S13        56   S9(10N)S10
S14        17   S13 AND S6 AND S7
S15       624   S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7 AND S8
S16         3   S1(10N)S2(10N)S3(10N)S4(10N) S5 (10N) S6 (10N)S7 (10N) S8
S17         3   S16 NOT S14
? show files
File 348:EUROPEAN PATENTS 1978-2002/Dec W03
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20021226,UT=20021219
         (c) 2002 WIPO/Univentio
?
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14/TI,AB,AD,AN,PN,PD/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Nonvolatile semiconductor storage device and test method therefor
Nichtfluchtige Halbleiterspeicheranordnung und Verfahren zu ihrer Prufung
Dispositif de memoire a semiconducteurs non-volatile et procede de test pour celui-ci
PATENT (CC, No, Kind, Date): EP 1176608 A2 020130 (Basic)
APPLICATION (CC, No, Date): EP 2001304985 010607;
PRIORITY (CC, No, Date): JP 2000176986 000613

ABSTRACT EP 1176608 A2
A control signal MBPRG is inputted to individual block decoders that constitute a block decoder section 37 of an ACT type flash memory. Then, the level of the control signal MBPRG is set to "H" to select all the blocks regardless of the contents of address signals a5 through a13, and one word line WL is selected from all the blocks by the addresses a0 through a4. By thus selecting one word line WL every block that is electrically separated by the select transistor and simultaneously applying a write voltage during the test to the same number of word lines WL as the number of blocks, the possible occurrence of a bad influence exerted on the other memory cells is prevented even when the memory cells in which a write operation during the test has been executed include a memory cell that has a negative threshold voltage.

14/TI,AB,AD,AN,PN,PD/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor memory device capable of multiple word-line selection and method of testing same
Halbleiterspeicherschaltung mit einem Selektor fur mehrere Wortleitungen, und Prufverfahren dafur
Dispositif de memoire muni d'un selecteur a multiples lignes de mots, et son procede de test
PATENT (CC, No, Kind, Date): EP 884735 A2 981216 (Basic)
EP 884735 A3 990324
APPLICATION (CC, No, Date): EP 98302797 980409;
PRIORITY (CC, No, Date): JP 97142314 970530; JP 982594 980108

ABSTRACT EP 884735 A2
A semiconductor memory device capable of conducting test operations includes a plurality of word drivers (34) which keep word lines (WL1 through WLn) in an active state when the word drivers (34) are selected until the word drivers (34) are reset. The semiconductor memory device further includes a control circuit (31, 32) which successively selects more than one of the plurality of word drivers (34) so as to achieve simultaneous activation of word lines (WL1 through WLn) corresponding to selected ones of the plurality of word drivers (34) during the test operations.

14/TI,AB,AD,AN,PN,PD/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

STAGGERED ROW LINE FIRING IN A SINGLE RAS CYCLE
VERSETZTER ZIELLEITUNGSBETRIEB IN EINEM EINZIGEN RAS-ZYKLUS
ACTIVATION DECALEE DE LIGNES DE MOTS DE RANGEES EN UN SEUL CYCLE D'IMPULSION DE SELECTION DE LIGNE
PATENT (CC, No, Kind, Date): EP 935802 A1 990818 (Basic)

EP 935802 B1 020123
WO 9820495 980514
APPLICATION (CC, No, Date): EP 97945588 971031; WO 97US19967 971031
PRIORITY (CC, No, Date): US 743476 961104

14/TI,AB,AD,AN,PN,PD/4 (Item 4 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Manufacturing defect analyzer
Herstellungsfehler Analysator
Analyseur de fautes de fabrication
PATENT (CC, No, Kind, Date): EP 714032 A2 960529 (Basic)
EP 714032 A3 970409
APPLICATION (CC, No, Date): EP 95307508 951023;
PRIORITY (CC, No, Date): US 329031 941025

ABSTRACT EP 714032 A2
A method for detecting faults on a printed circuit board populated with semiconductor electronic components. To detect faults, signal pins on the components are taken in pairs. The an indication of the common mode resistance between those pins and ground is computed from a series of current measurements. An error is detected when the common mode resistance is outside of a predetermined range. A "learn mode" is also disclosed in which the pairs of leads used for the test are selected by taking measurements on a known good board without detailed knowledge of the semiconductor components on the board. (see image in original document) (see image in original document)

14/TI,AB,AD,AN,PN,PD/5 (Item 5 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Logic circuit using PLA for synchronous dual word coding
Logikschaltung mit einem programmierbaren logischen Feld fur eine synchrone Kodierung von doppelten Wortern
Circuit logique utilisant un reseau logique programmable pour codage synchrone de mots doubles
PATENT (CC, No, Kind, Date): EP 673119 A1 950920 (Basic)
EP 673119 B1 991020
APPLICATION (CC, No, Date): EP 95301414 950306;
PRIORITY (CC, No, Date): US 214529 940318

ABSTRACT EP 673119 A1
A logic circuit arrangement for performing synchronous dual word decoding utilizing a programmable logic array which is formed with a reduced number of transistor counts. This is achieved by organizing the AND plane (64) so as to decode only the seven (7) most significant bits of an 8-bit opcode word. A LSB decoder circuit (153) is used for decoding the least significant bit of the opcode word separately and outside of the AND plane. As a result, the amount I.C. chip space required has been substantially reduced. (see image in original document)

14/TI,AB,AD,AN,PN,PD/6 (Item 6 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Testing variably controllable delay units.
Testen variabel einstellbarer Verzogerungseinheiten.
Test d'unites de retard a reglage variable.

PATENT (CC, No, Kind, Date): EP 671633 A2 950913 (Basic)
EP 671633 A3 960821
APPLICATION (CC, No, Date): EP 95301174 950223;
PRIORITY (CC, No, Date): US 209819 940311

ABSTRACT EP 671633 A3
A test configuration is provided which allows a plurality of variable delay units (106) within a delay chain to be compared with respect to one another. The delay chain is employed within a clock generator circuit that generates internal clock signals of a microprocessor. During normal operation, a set of multiplexers (202) interposed within the delay chain are configured such that the plurality of variable delay units are electrically coupled in series with respect to one another. During a test operation when it is desired to test the variable delay units for possible defects, the four delay units are electrically separated from one another by setting the multiplexers in a test mode. A common test signal is then driven through two or more of the variable delay units simultaneously, and a compare circuit coupled to the output of each variable delay unit determines whether a transition in the common pulse signal propagated through each variable delay unit at essentially the same time. If no manufacturing defects are present, the four outputs of the variable delay units should be virtually indistinguishable from one another. Similar tests may be conducted throughout the entire operating range of the variable delay units. (see image in original document)

14/TI,AB,AD,AN,PN,PD/7 (Item 7 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Configuration and method for testing a delay chain within a microprocessor clock generator.
Konfiguration und Verfahren zur Prufung einer Verzogerungsleitung in einen Mikrorechner-Taktgenerator.
Configuration et procede pour tester une ligne a retard dans un generateur de signaux d'horloge d'un microprocesseur.
PATENT (CC, No, Kind, Date): EP 671688 A2 950913 (Basic)
EP 671688 A3 980812
APPLICATION (CC, No, Date): EP 95301173 950223;
PRIORITY (CC, No, Date): US 212037 940311

ABSTRACT EP 671688 A2
A test configuration is provided which allows a plurality of variable delay units within a delay chain of a microprocessor clock generator to be compared with respect to one another. During normal operation. a set of multiplexers interposed within the delay chain are configured such that the plurality of variable delay units are electrically coupled in series with respect to one another. An external command signal may be provided to the microprocessor to initiate a test operation in which the variable delay units are tested for possible defects. During the test operation, a control unit selects the multiplexers such that the four delay units are electrically separated from one another. A common test signal is then driven through two or more of the variable delay units simultaneously. and a compare circuit coupled to the output of each variable delay unit determines whether a transition in the common pulse signal propagated through each variable delay unit at essentially the same time. If no manufacturing defects are present, the four outputs of the variable delay units should be virtually indistinguishable from one another. The results of the compare operation may be driven on external pins of the microprocessor or may be processed internally within the microprocessor. Similar tests may be conducted throughout the entire

operating range of the variable delay units. (see image in original document)

14/TI,AB,AD,AN,PN,PD/8 (Item 8 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

System scan path architecture
Architektur des Abtastpfads eines Systems
Architecture de trajet d'analyse d'un systeme
PATENT (CC, No, Kind, Date): EP 417905 A2 910320 (Basic)
EP 417905 A3 920408
EP 417905 B1 971105
APPLICATION (CC, No, Date): EP 90308724 900808;
PRIORITY (CC, No, Date): US 391801 890809; US 391751 890809

ABSTRACT EP 417905 A2
A system scan path architecture is provided by a device select module (DSM) (18) which may be used in conjunction with associated circuits (16a-b) to select secondary scan paths (PATH1-m) on each circuit for coupling with a primary scan path on a test bus (14). The test bus (14) is controlled by a primary bus master (12). Remote bus masters may be used in conjunction with the DSMs (18) to provide serial-scan testing independent of the primary bus master (12). (see image in original document)

14/TI,AB,AD,AN,PN,PD/9 (Item 9 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Pressure calibration reference, e.g. for a syringe.
Referenzdruckerzeuger, z.B. in Form einer Injektionsspritze.
Etalon de pression realise par seringue.
PATENT (CC, No, Kind, Date): EP 316763 A1 890524 (Basic)
EP 316763 B1 920819
APPLICATION (CC, No, Date): EP 88118726 881110;
PRIORITY (CC, No, Date): US 120874 871116

ABSTRACT EP 316763 A1
A compact, inexpensive, and lightweight pressure calibrator (10) comprises a plunger (14) sized to slide snugly within a hypodermic syringe barrel (12). Included within the plunger are a pressure transducer (56), a microprocessor (54) and other electronic components (62). A digital display (30) disposed within the side of the plunger is operative to display the pressure developed within the syringe barrel (12) as the operator moves the plunger. "O" rings (28) provide a hermetic seal between the plunger and the internal bore (16) of the syringe barrel. A tube (22) is **connected** to the output port (20) of the syringe and provides fluid communication between the syringe and a pressure monitoring device (26) being calibrated.

14/TI,AB,AD,AN,PN,PD/10 (Item 10 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Television signal generator.
Fernsehsignalerzeuger.
Generateur de signal de television.
PATENT (CC, No, Kind, Date): EP 260658 A2 880323 (Basic)
EP 260658 A3 900117

EP 260658 B1 940427
APPLICATION (CC, No, Date): EP 87113479 870915;
PRIORITY (CC, No, Date): US 908553 860917

ABSTRACT EP 260658 A2
A television signal generator which is fully digital has digital data stored in PROMs, one PROM for each component of the desired encoded television signal corresponding to luminance data and chrominance data. A system clock allows a signal address generator to fetch data from the PROMs. The chrominance data from the PROMs is mixed with appropriate digital representations of a sinusoidal function and a phase offset and is added to the luminance data. The combined digital signal is converted to analog, filtered and output as the desired encoded television signal.

14/TI,AB,AD,AN,PN,PD/11 (Item 11 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Cochlear implant system with psychological testing or programming with mapped patient responses provided to encoder.
Cochleares Implantationssystem mit psychologischem Testen oder Programmieren mittels kartographierter Reaktionen des Patienten, vorgesehen zur Codierung.
Systeme implantable cochleaire avec tests ou programmations psychologiques par l'intermediaire des reponses cartographiques du malade prevues pour le codage.
PATENT (CC, No, Kind, Date): EP 241101 A1 871014 (Basic)
EP 241101 B1 920916
APPLICATION (CC, No, Date): EP 87200716 840409;
PRIORITY (CC, No, Date): US 483806 830411

ABSTRACT EP 241101 A1
A cochlear implant system having a speech processor located external to a patient's body, said speech processor including sound-to-stimulation encoding means, a body-implantable receiver-stimulator and an electrode array implantable in the cochlea of a patient for receiving electrical signals from said encoding means, whereby
means for performing psychophysical testing on the auditory nervous system of the patient while said receiver-stimulator is receiving said electrical signals,
means, using the results of said testing, for preparing data in a map representing a patient stimulation strategy;
means for converting audio signal information to electrical signals in said sound-to-stimulation encoding means for that patient; and
means for erasably programming and storing said mapped data in said encoding means, such that stimulation parameters for speech signals are optimized utilizing said stored data to enhance the ability of the patient to recognize speech signals.

14/TI,AB,AD,AN,PN,PD/12 (Item 12 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Semiconductor memory device.
Halbleiterspeichergerat.
Dispositif de memoire a semi-conducteur.
PATENT (CC, No, Kind, Date): EP 249903 A2 871223 (Basic)
EP 249903 A3 891025
EP 249903 B1 920513

APPLICATION (CC, No, Date): EP 87108508 870612;
PRIORITY (CC, No, Date): JP 86136838 860612

ABSTRACT EP 249903 A2
A semiconductor memory device includes a main memory cell array (30A), a redundancy memory cell array (30B), **bonding** pads for receiving an address signal, a row decoder (32) for selecting a row of the main memory cell array (30A), in accordance with the row address signal, and an exchange controller (46) **connected** to receive the address signal, which is programmable to inhibit the selective operation of the row decoder (32) to select the row of the redundancy memory cell array (32B), in response to specific address signals. The semiconductor memory device further includes **bonding** pads each for receiving a test signal. The exchange controller (46) is **connected** to receive the test signal for inhibiting the selective operation of the row decoder (32) and selecting the row of the redundancy memory cell array (30B), in response to the test signal.

14/TI,AB,AD,AN,PN,PD/13 (Item 13 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Shift register latch arrangement for enhanced testability in differential cascode voltage switch circuit.
Schieberegistersignalspeicheranordnung zur erhohten Prufbarkeit in differentialer Kaskadenspannungsschalterschaltung.
Agencement de bascule de maintien de registre a decalage a testabilite accrue dans un circuit de commutation de tension en cascade differentiel.
PATENT (CC, No, Kind, Date): EP 240719 A2 871014 (Basic)
EP 240719 A3 891129
EP 240719 B1 920122
APPLICATION (CC, No, Date): EP 87103051 870304;
PRIORITY (CC, No, Date): US 850189 860410

ABSTRACT EP 240719 A2
A shift register latch (SRL) arrangement for testing a combinational logic circuit, producing true and complement outputs in nature, has two clocked DC latches (32, 34) and additional circuitry (36) for providing an input to the second latch. Clock signal trains (A, B, C) and an extra TEST signal (44) are used to control the SRL arrangement in different modes. In a first mode, one of the outputs (30) from the combinational logic circuit is latched into the first latch and provided to a succeeding combinational logic circuit. In a second mode, a plurality of the SRL arrangements are interconnected together to form a shift register chain so that each latch acts as one position of the shift register chain. Further, in a third mode, the true (30) and complement (38) outputs of the combinational logic circuit are exclusive ORed and its result is latched into the second latch. During the third mode, output of the first latch is prevented from being latched into the second latch.

14/TI,AB,AD,AN,PN,PD/14 (Item 14 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

CRC calculation machines.
CRC-Rechenmaschinen.
Machines pour calculer les CRC.
PATENT (CC, No, Kind, Date): EP 230730 A2 870805 (Basic)
EP 230730 A3 900314

EP 230730 B1 931110
APPLICATION (CC, No, Date): EP 86309177 861125;
PRIORITY (CC, No, Date): US 803367 851202

ABSTRACT EP 230730 A2
There is disclosed herein a CRC calculation circuit which can calculate CRC checkbits on 8 bits of raw input data per cycle of a byte clock. The calculation apparatus uses 8 rows of shifting links with the inputs of each row coupled to the data outputs of the preceding row. Each shifting link shifts its input bit one bit position toward the most significant bit, and selected shifting links perform an exclusive-OR operation (84) between their input bits and the output of an input exclusive-OR gate which exclusive-OR's (84) one input bit with one of the bits in the most significant byte of the checksum register (30). A byte wide output (70) bus is used to access the final checkbits from the checksum register (30) by disabling the array of shifting links during the output cycles so that the bytes of CRC data can be shifted into position through the array one byte per each cycle of the byte clock. Preset logic for forcing all logic 1's into the data inputs of the first row of shifting links is provided such the machine can be preset during the first clock cycles of the CRC calculation. Several differenct architectures are disclosed for allowing separate calculation of CRC bits on a header packet and a data packet where the CRC bits on the data packet may be calculated on the data alone or the data plus the header and the CRC bits for the header. Logic for allowing CRC calculation to be performed on all bytes of a message while excluding some selected number of bits in the first byte is also disclosed.

14/TI,AB,AD,AN,PN,PD/15 (Item 15 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

CRC calculation machine and method for CRC calculation.
CRC-Rechenmaschine und Methode zur CRC-Berechnung.
Machine et methode pour calculer les CRC.
PATENT (CC, No, Kind, Date): EP 225763 A2 870616 (Basic)
EP 225763 A3 900314
EP 225763 B1 931110
APPLICATION (CC, No, Date): EP 86309175 861125;
PRIORITY (CC, No, Date): US 803366 851202

ABSTRACT EP 225763 A2
There is disclosed herein a CRC calculation circuit which can calculate CRC checkbits on 8 bits of raw input data per cycle of a byte clock. The calculation apparatus uses 8 rows of shifting links with the inputs of each row coupled to the data outputs of the preceding row. Each shifting link shifts its input bit one bit position toward the most significant bit, and selected shifting links perform an exclusive-OR operation between their input bits and the output of an input exclusive-OR gate which exclusive-OR's (84) one input bit with one of the bits in the most significant byte of the checksum register (30). A byte wide output bus (8) is used to access the final checkbits from the checksum register (30) by disabling the array of shifting links during the output cycles so that the bytes of CRC data can be shifted into position through the array one byte per each cycle of the byte clock. Preset logic for forcing all logic 1's into the data inputs of the first row of shifting links is provided such the machine can be preset during the first clock cycle of the CRC calculation. Several differenct architectures are disclosed for allowing separate calculation of CRC bits on a header packet and a data packet where the CRC bits on the data packet may be calculated on the data alone or the data plus the header and the CRC bits for the header. Logic for

allowing CRC calculation to be performed on all bytes of a message while excluding some selected number of bits in the first byte is also disclosed.

14/TI,AB,AD,AN,PN,PD/16 (Item 16 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Digital envelope shaping apparatus.
Digitales Hullkurvenformgebungsgerat.
Appareil numerique de mise en forme d'enveloppe.
PATENT (CC, No, Kind, Date): EP 220059 A2 870429 (Basic)
EP 220059 A3 890726
EP 220059 B1 911106
APPLICATION (CC, No, Date): EP 86308005 861015;
PRIORITY (CC, No, Date): US 789069 851017; US 853304 860417

ABSTRACT EP 220059 A2
A system for forming digital synchronization signals suitable for insertion in a television signal comprises a first number generator (26) generating digital signals which represent the peak amplitudes of the desired synchronization signals, a second number generator (28) which synchronously generates digital signals respresenting the shape of the edges of the synchronization signals and a multiplier (20) which during an appropriate blanking interval multiplies the signals from the generators.

14/TI,AB,AD,AN,PN,PD/17 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

FLASH MEMORY ARRAY
ENSEMBLE MEMOIRE FLASH
Patent and Priority Information (Country, Number, Date):
Patent: WO 9916077 A1 19990401
Application: WO 98US19326 19980916 (PCT/WO US9819326)

English Abstract
A novel flash memory array has an array of memory cells (41a, 40b) with each memory cell being of a floating gate memory transistor with a plurality of terminals. The memory cells (40a, 40b) are arranged in a plurality of rows and a plurality of columns, with a word line **connecting** the memory cells in the same row. A row decoder (44) is positioned adjacent one side of the memory array and is **connected** to the plurality of word lines for receiving an address signal and for supplying a low voltage signal. A plurality of programming lines (D0-D7) are **connected** to the plurality of rows of memory cells (41a, 41b) of the array with a programming line **connected** to the memory cells in the same row. The plurality of programming lines (D0-D7) are collinear with but spaced apart from the plurality of word lines and extending only to the row decoder (44). A high voltage generating circuit (100) is positioned adjacent the other side of the array, opposite the one side, and **connected** to the plurality of programming lines (D0-D7) for receiving the address signal and for supplying a high voltage signal to the plurality of programming lines in response thereto.

French Abstract
Nouvelle memoire flash possedant un ensemble de cellules de memoire (41a, 40b) consistant chacune en un transistor de memoire a grille flottante comportant une pluralite de bornes. Ces cellules de memoires

(40a, 40b) sont disposees en une pluralite de rangees et de colonnes, une ligne de mots reliant les cellules de memoire de la meme rangee. Un decodeur (44) de rangee est place contigu a un cote de l'ensemble memoire et est relie a la pluralite de lignes de mots afin de recevoir un signal d'adresse et de generer un signal de basse tension. Une pluralite de lignes de programmation (DO-D7) est reliee a la pluralite de rangees de cellules de memoire (41a, 41b) de l'ensemble, une ligne de programmation etant reliee aux cellules de memoire de la meme rangee. La pluralite de lignes de programmation (D0-D7) est colineaire par rapport a la pluralite de lignes de mots, mais eloignee de celle-ci, et s'etend seulement vers le decodeur (44) de rangee. Un circuit (100) de generation de haute tension est place contigu a l'autre cote de l'ensemble, en face du premier cote, et relie a la pluralite de lignes de programmation (D0-D7) afin de recevoir le signal d'adresse et de transmettre un signal de haute tension en reaction a la pluralite de lignes de programmation.

?

17/TI,AB,AD,AN,PN,PD,K/1 **(Item 1 from file: 348)**
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

BUS FOR SENSITIVE ANALOG SIGNALS
BUS FUR EMPFINDLICHE ANALOGE SIGNALE
BUS POUR SIGNAUX ANALOGIQUES SENSIBLES
PATENT (CC, No, Kind, Date): EP 784799 A1 970723 (Basic)
EP 784799 B1 981125
WO 9611411 960418
APPLICATION (CC, No, Date): EP 95932598 951003; WO 95CA560 951003
PRIORITY (CC, No, Date): US 318950 941006

...SPECIFICATION This invention relates to a testability structure and more particularly to an analog test access **bus** for analog or mixed analog/digital integrated circuits (ICs).

Background of the Invention
As the...

...are in one of two modes: high or low, and hence the ramifications of applying **test** conditions to such circuits are less severe. Consequently, **test** procedures for digital circuits are well developed. Analog circuits, on the other hand, are influenced...
...etc. Therefore, testability structure which permits any of these elements to be introduced to a **test** **node** on an analog circuit will result in inaccurate **test** data. In an integrated circuit it is known to employ an analog bus to convey signals originating inside the IC to an output pin for **evaluation** .

Prior Art
One known structure for **testing** analog signals is illustrated in FIGURE 1. The structure comprises one or more on-chip CMOS transmission gates which convey the **test** signals off chip through an electro-static discharge (ESD) protection network. A **tester** is **connected** either directly to the **test** pad or to the **test** pad via an off-chip amplifier (not shown). This structure is relatively simple and consumes little extra silicon area on the IC. The bandwidth is limited primarily by the output **impedance** of the source **node** under test, the resistance of the transmission gate, the resistance of the ESD network and...

...structure according to the prior art is illustrated in FIGURE 2. In this configuration the **signal** of interest is connected to the analog bus via a CMOS transmission gate and conveyed...

17/TI,AB,AD,AN,PN,PD,K/2 **(Item 1 from file: 349)**
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

TDR LAN CABLES ATTENUATION MEASUREMENT
MESURE D'AFFAIBLISSEMENT ASYMETRIQUE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200207419 A2-A3 20020124 (WO 0207419)
Application: WO 2001US22068 20010713 (PCT/WO US0122068)

English Abstract
A signal-based cable attenuation measurement device, system and methodology provides measurement of attenuation characteristics of a cable over a wide frequency spectrum. Located at a single location on a cable, a measurement device injects a signal on to the cable under measurement and receives the reflected signal, recording physical

characteristics of the cable in response to the signal. A model, calibrated to estimate the effects of the cable with know impedances, evaluates the waveform generated from the cable's response to the signal and computes attenuation of the cable as a function of frequency. In some circumstances, when low signal-to-noise effects result, normally at high frequencies in long cables, the attenuation of the cable is further fitted to the model to correct the errors that occur as a result of the low signal-to-noise effects.

French Abstract

L'invention concerne un dispositif, un systeme et une methodologie de mesure d'affaiblissement de cable a base de signal permettant de mesurer des caracteristiques d'affaiblissement d'un cable sur un large spectre de frequences. Place en un endroit sur le cable, ledit dispositif de mesure injecte un signal dans le cable a mesurer et recoit le signal reflechi, les caracteristiques physiques du cable en reponse au signal etant enregistrees. Un modele, etalonne pour estimer les effets du cable avec des impedances connues, permet d'evaluer la forme d'onde generee a partir de la reponse du cable au signal et de calculer l'affaiblissement du cable en fonction de la frequence. Dans certains cas, lorsque des effets signal/bruit faibles se produisent, d'ordinaire a des frequences elevees dans de longs cables, l'affaiblissement du cable est encore adapte au modele afin de corriger les erreurs qui surviennent par suite des effets signal/bruit faibles.

Fulltext Availability:

Detailed Description

Detailed Description

... of the signal as it propagates along portion 234. The digitizer creates a sample data **array** for wavefonn 204 at discrete time intervals. The data sample comprising waveform 204 comprises a...

...to a single end of cable 230 in place of either network device 16 or **nodes** 1612. The **testing** environment for the alternative embodiment is shown in Fig. 4D. In such an environment, no...

...side portion 232 with impedance 236 to isolate the hub side portion with a known **impedance** is eliminated in steps 218, 220, 222 and 240. Fig. 4E illustrates the calibration configuration to sample waveforms 202 when measurement 50 resides on a single end of **cable** 230. Measurement device 50 resides at a single end of **cable** 230 in place of the network device or the **nodes** that would otherwise normally be connected at the **cable** 's end in an operating network. In place of **cable** 230, **impedances** 238 are **connected** to **measurement** device 50. Steps 218, 220, and 222 of ...described in Fig 5 are thereafter performed, except for the step of connecting resistors 236, **impedance** Zh is eliminate, and the resulting waveforms 202 sampled. In the same manner, data acquisition step 240 is performed, except that the process of connecting **impedance** Zh 236 is eliminated and the remaining aspects of the data acquisition process continue in the **testing** environment shown in Fig 4F to sample **cable** waveform 204.

[00701 An exemplary response of wavefonn 204 as measured at point M is...

...in voltage resulting in sloping effect to waveform 204 as the reflected component of the **signal** returns the cable's length.

[00711 Upon sampling waveforra 204, the sampled waveform data, Vc...

17/TI,AB,AD,AN,PN,PD,K/3 (Item 2 from file: 349)

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BUS FOR SENSITIVE ANALOG SIGNALS
BUS POUR SIGNAUX ANALOGIQUES SENSIBLES

Patent and Priority Information (Country, Number, Date):
Patent: WO 9611411 A1 19960418
Application: WO 95CA560 19951003 (PCT/WO CA9500560)

English Abstract
A bus structure for sensitive analog signals suitable for testability in integrated circuits. The structure incorporates one or more simple 3-state inverters each having a first input for receiving test data from a node of interest and a second input selectively supplied with an enabling signal to initiate a test mode. The output of the 3-state inverter is connected to an operational amplifier circuit via a common analog bus. The operational amplifier circuit maintains the bus at a substantially constant voltage. The output voltage of the operational amplifier will be approximately linearly proportional to the test data.

French Abstract
La presente invention concerne une structure de bus pour signaux analogiques sensibles permettant d'effectuer des tests au niveau des circuits integres. La structure incorpore un ou plusieurs inverseurs a trois etats, chacun de ces inverseurs disposant, d'une part,d'une premiere entree pour la reception des donnees de test d'un noeud a examiner, et d'autre part, d'une seconde entree pour la prise en compte d'un signal de validation lancant le mode test. La sortie de l'inverseur a trois etats est connectee a un amplificateur operationnel via un bus analogique commun. Cet amplificateur operationnel maintient le bus a une tension sensiblement constante. La tension de sortie de l'amplificateur operationnel est normalement une fonction approximativement lineaire des donnees de test.

Fulltext Availability:
Detailed Description

Detailed Description
BUS FOR SENSITIVE ANALOG SIGNALS
Field of invention
This invention relates to a Lestability structure and...

...are in one of two modes: high or low, and hence the ramifications of applying **test** conditions to such circuits are less severe. Consequently, **test** procedures for digital circuits are well developed.

Analog circuits, on the other hand, are influenced...

...etc. Therefore, testability structure which permits any of these elements to be introduced to a **test** **node** on an analog circuit will result in inaccurate **test** data. In an integrated circuit it is known to employ an analog bus to convey signals originating inside the IC to an output pin for **evaluation** .

Prior Art
One known structure for **testing** analog signals is illustrated in FIGURE 1. The structure comprises one or more on-chIp CMOS transmission gates which convey the **test**

signals off chip through an electro-static discharge (ESD) protection network. A **tester** is **connected** either directly to the **test** pad or to the **test** pad via an off-chip amplifier (not shown). This structure is relatively simple and consumes little extra silicon area on the IC. The bandwidth is limited primarily by the output **impedance** of the source **node** under test, the resistance of the transmission gatep the resistance of the ESD network and...

...additional
disadvantage of this structure is that the bandwidth is limited and may be only **several** MHz for practical resistances, say, 1KQ - 5KQ and capacitances of 2OpF 5OpF. The structure Of...
?

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Set     Items   Description
S1        306   AU=(ROMERO G? OR ROMERO, G? OR SCHMITZ W? OR SCHMITZ, W? OR
               PAULSEN, E? OR PAULSEN E?)
S2    2582969   SIGNAL? ?
S3    2798991   TEST???? OR EXAMIN????? OR CHECK???? OR ANALY???? OR INSPE-
               CT???? OR EVALUAT?
S4      84975   S2(2N)S3
S5          1   S4 AND S1
S6         16   S1 AND S2 AND S3
S7         15   S6 NOT S5
S8    3371158   CABLE? OR LINES OR LINE OR WIRE? ? OR LEAD? ? OR BUS??
S9         11   S7 AND S8
S10        11   IDPAT (sorted in duplicate/non-duplicate order)
S11        10   IDPAT (primary/non-duplicate records only)
? show files
File 347:JAPIO Oct 1976-2002/Aug(Updated 021203)
         (c) 2002 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2002/Dec W03
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20021226,UT=20021219
         (c) 2002 WIPO/Univentio
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200282
         (c) 2002  Thomson Derwent
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5/9,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009804336 **Image available**
WPI Acc No: 1994-084191/199411
XRPX Acc No: N94-065860
Fault recognition system for information transmission device - evaluates **carrier** signals **received from peripherals in response to each interrogation call**
Patent Assignee: SIEMENS AG (SIEI)
Inventor: KARL R; KECK R; **SCHMITZ W**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4229212	A1	19940310	DE 4229212	A	19920904	199411	B

Priority Applications (No Type Date): DE 4229212 A 19920904
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4229212	A1		7	G08C-025/00	

Abstract (Basic): DE 4229212 A
The fault recognition system uses a information transmission device having an interrogation unit (3) associated with a given number of peripherals (7a....7n) for two-way communication via a barrier signal. The fault recognition system allows the carrier signal received by the interrogation unit in response to each interrogation call to be evaluated.
When an abnormal carrier signal is detected, a fault signal is supplied to the peripherals, for initiating a selection routine allowing the fault to be located. Pref. the fault signal is supplied as a fault telegram, as a multiple repetition of the call signal, or as a suppression of all call signals over a timed interval.
ADVANTAGE - Rapid identification and location of fault.
Dwg.1/3
Title Terms: FAULT; RECOGNISE; SYSTEM; INFORMATION; TRANSMISSION; DEVICE; EVALUATE; CARRY; SIGNAL; RECEIVE; PERIPHERAL; RESPOND; INTERROGATION; CALL
Derwent Class: T01; W01; W05; X12
International Patent Class (Main): G08C-025/00
International Patent Class (Additional): H02J-013/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-G05; W01-A03; W01-A06A2; W05-D05C; X12-H03A

... evaluates **carrier** signals **received from peripherals in response to each interrogation call**
...Inventor: **SCHMITZ W**